

## CLAIMS

What is claimed is:

- 1 1. An apparatus, comprising:  
2 a state-machine-based network protocol unit disposed on an integrated  
3 circuit, the network protocol unit having state machines to control other units of the  
4 integrated circuit and to process a network protocol corresponding to data  
5 throughput through the integrated circuit; and  
6 a storage unit disposed on the integrated circuit and coupled to the network  
7 protocol unit, the storage unit responsive to the network protocol unit to store and to  
8 control direction of the data throughput through the integrated circuit.
- 1 2. The apparatus of claim 1 wherein the storage unit comprises:  
2 a first buffer to temporarily store data throughput through the integrated circuit  
3 in a first direction;  
4 a second buffer to temporarily store data throughput through the integrated  
5 circuit in a second direction different from the first direction; and  
6 a controller coupled to the first and second buffers and responsive to the  
7 state machines to determine which of the first or second buffers forward their  
8 respective stored data.
- 1 3. The apparatus of claim 1 wherein the network protocol unit comprises part of  
2 a packet processor unit, the packet processor unit including:  
3 an initialization unit to read information external to the integrated circuit and to  
4 use that information to program the state machines; and

5 a packet assembler interface through which to provide commands related to  
6 data throughput within the integrated circuit.

1 4. The apparatus of claim 3, further comprising a packet assembler unit  
2 disposed on the integrated circuit and coupled to the packet assembler interface to  
3 receive the commands, the packet assembler unit responsive to the commands to  
4 retrieve data and to assemble a packet having header information and the retrieved  
5 data.

1 5. The apparatus of claim 3, further comprising a state-machine-based network  
2 device control component disposed on the integrated circuit and coupled to the  
3 packet processor unit, the network device control component having state machines  
4 to control transmission of packet data from the integrated circuit to a network device  
5 and reception of packet data from the network device to the integrated circuit.

1 6. The apparatus of claim 5 wherein the network device control component  
2 includes:

3 an arbiter to arbitrate for bus use associated with the transmission and the  
4 reception of the packet data;

5 a first controller having logic to determine direction of the packet data; and

6 a second controller having logic to perform bus protocol associated with the  
7 packet data.

1 7. The apparatus of claim 4, further comprising a port controller disposed on the  
2 integrated circuit and coupled to the packet processor unit, the port controller being

3 capable to control transmission of data from the integrated circuit to an appliance  
4 and reception of data from the appliance to the integrated circuit.

1 8. The apparatus of claim 3, further comprising a controller disposed on the  
2 integrated circuit and coupled to the initialization unit, the controller having an  
3 interface to receive the external information to program the state machines and to  
4 provide the received external information to the initialization unit.

1 9. The apparatus of claim 5 wherein the state machines of the network device  
2 control component include:

3 a first state machine to interface the network device control component to the  
4 network device;

5 a second state machine to control reception of packet data sent from the  
6 network device to the integrated circuit; and

7 a third state machine to control transmission of packet data sent from the  
8 integrated circuit to the network device.

1 10. The apparatus of claim 4 wherein the state machines include:

2 a first state machine associated with the packet processor unit to control  
3 processing of the data throughput through the integrated circuit; and

4 a second state machine associated with the packet assembler unit to control  
5 assembly of the packet.

1 11. A system, comprising:

2 an appliance;

3 a network device; and

4' an integrated circuit coupled between the appliance and the network device  
5 to receive data transmitted between the appliance and the network device, the  
6 integrated circuit including:

7 a state-machine-based packet processor unit having state-machines to  
8 control other units of the integrated circuit and to process a network protocol  
9 corresponding to data throughput through the integrated circuit; and

10 a storage unit coupled to the packet processor unit and responsive to  
11 the packet processor unit to store and to control direction of the data  
12 throughput through the integrated circuit.

1 12. The system of claim 11 wherein the appliance comprises a printer device.

1 13. The system of claim 11 wherein the storage unit comprises:

2 a first buffer to temporarily store data throughput through the integrated circuit  
3 from the appliance to the network device;

4 a second buffer to temporarily store data throughput through the integrated  
5 circuit from the network device to the appliance; and

6 a controller coupled to the first and second buffers and responsive to the  
7 state machines to determine which of the first or second buffers forward their  
8 respective stored data.

1 14. The system of claim 11 wherein the packet processor unit includes an  
2 initialization unit to read information external to the integrated circuit and to use that  
3 information to program the state machines, the system further comprising a storage  
4 device external to the integrated circuit having the external information stored  
5 therein and readable by the initialization unit.

1 15. The system of claim 11 wherein the integrated circuit further comprises:  
2 a packet assembler unit coupled to the packet processor unit to receive  
3 commands related to data throughput within the integrated circuit, and being  
4 responsive to the commands to retrieve data and to assemble a packet having  
5 header information and the retrieved data; and  
6 a state-machine-based network device control component coupled to the  
7 packet processor unit and to the packet assembler unit, the network device control  
8 component having state machines to control transmission of packet data from the  
9 integrated circuit to the network device and reception of packet data from the  
10 network device to the integrated circuit.

1 16. A method, comprising:  
2 using state machines disposed on an integrated circuit to process network  
3 protocol information associated with data receivable by the integrated circuit;  
4 determining a destination of the data using the state machines;  
5 storing the data in a storage unit disposed on the integrated circuit and  
6 forwarding the stored data from the storage unit to the destination based on a  
7 command from the state machines.

1 17. The method of claim 16, further comprising:  
2 using the state machines to issue a command related to a request for data;  
3 in response to the command, assembling a packet having header information  
4 and the requested data; and  
5 transmitting the assembled packet to a network device that requested the  
6 data via a state-machine-based bus protocol controller.

1 18. The method of claim 16, further comprising programming the state machines  
2 using information stored externally to the integrated circuit and loaded on to the  
3 integrated circuit during power up.

1 19. The method of claim 17 wherein the state machines include:  
2 a first state machine to control processing of the command related to the  
3 request for data; and  
4 a second state machine to control assembly of the packet having the header  
5 information and the requested data.

1 20. The method of claim 16 wherein the state machines include:  
2 a first state machine to interface the integrated circuit to a network device;  
3 a second state machine to control reception of data sent from the network  
4 device to the integrated circuit; and  
5 a third state machine to control transmission of data sent from the integrated  
6 circuit to the network device.